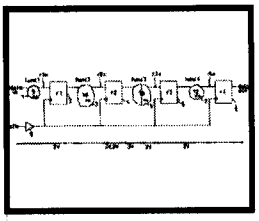
Derwent Record

Derwent Title: **Logic synthesis for low power combinatorial SIC - involves mapping combinatorial circuit onto circuits driven by high and low voltages when circuit has delay above design limit providing circuit with delay below limit**

Original Title: EP0744704A2: Logic synthesis method, semiconductor integrated circuit and arithmetic circuit



Assignee: **MATSUSHITA DENKI SANGYO KK** Standard company
Other publications from MATSUSHITA DENKI SANGYO KK (MATU)...
MATSUSHITA ELEC IND CO LTD Standard company
Other publications from MATSUSHITA ELEC IND CO LTD (MATU)...
MATSUSHITA ELECTRIC IND CO LTD Standard company
Other publications from MATSUSHITA ELECTRIC IND CO LTD (MATU)...

Inventor: **KAZUTAKE O; OHARA K;**

Accession/ Update: **1997-001436 / 200564**

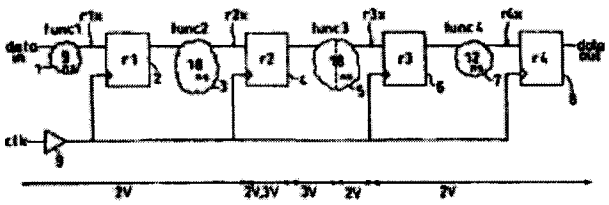
IPC Code: **G06F 1/32 ; G06F 17/50 ; H01L 27/04 ; H03K 19/00 ;** G06F 7/48 ; G06F 7/50 ; G06F 7/52 ; H01L 21/82 ; H01L 21/822 ; H03K 19/0175 ; H03K 19/20 ;

Derwent Classes: T01;

Manual Codes: **T01-J15A3**(Computer simulation of electrical and electronic circuits)

Derwent Abstract: (EP0744704A) The logic synthesis method involves mapping the combinatorial circuit into circuit driven by low voltage when circuit has delay above design upper limit. A part of the combinatorial circuit is then mapped into a circuit driven by a high voltage. The remaining part of the combinatorial circuit is mapped into a circuit of the first type ensuring the circuit has a delay below the signal propagation delay upper limit.
If the first step produces a combinatorial circuit of the first and second types arranged so that the output from the first circuit is the input to the second then the first circuit is remapped into the second type. It is determined which of the registers provides a signal to the mapped or remapped second circuits. A register providing a signal to the second combinatorial circuit is mapped into a register driven by a voltage source including a high level voltage source. A register found to provide no signal to the second combinational circuit is mapped into a register driven by a low voltage.
Advantage - Facilitates low power SIC generation with no increase in delay time of critical paths contained in combination circuits of SIC. Provides low power SIC with out increasing critical path delay time.

Images:



Dwg.13/42

Family:

PDF	Patent	Pub. Date	Derwent Update	Pages	Language	IPC Code
	EP0744704A2 *	1996-11-27	199701	62	English	G06F 17/50
	Des. States: (R) DE FR GB IT NL					
	Local appls.: EP1996000108359 Filed:1996-05-24 (96EP-0108359)					
	CN1130829C =	2003-12-10	200564		English	H03K 19/00
	Local appls.: CN1996000107886 Filed:1996-05-24 (96CN-0107886)					
	CN1430331A =	2003-07-16	200363		English	H03K 19/00
	Local appls.: CN2002000152829 Filed:1996-05-24 (2002CN-0152829) Div ex CN1996000107886 Filed:1996-05-24 (96CN-0107886)					
	DE69623688E =	2002-10-24	200278		German	G06F 17/50
	Local appls.: Based on EP00744704 (EP 744704) EP1996000108359 Filed:1996-05-24 (96EP-0108359) DE1996000623688 Filed:1996-05-24 (96DE-0623688)					
	EP0744704B1 =	2002-09-18	200269	64	English	G06F 17/50
	Des. States: (R) DE FR GB IT NL					
	Local appls.: Related to EP00955594 (EP 955594) EP1996000108359 Filed:1996-05-24 (96EP-0108359) Related to EP1999000113174 Filed:1996-05-24 (99EP-0113174)					
	KR0296183B =	2001-10-22	200236		English	G06F 17/50
	Local appls.: Previous Publ. KR96043163 (KR 96043163) KR1996000015991 Filed:1996-05-14 (96KR-0015991)					
	US5978573 =	1999-11-02	199953	53	English	G06F 17/50
	Local appls.: US1998000172705 Filed:1998-10-15 (98US-0172705) Div ex US1996000653651 Filed:1996-05-24 (96US-0653651)					
	JP11274413A2 =	1999-10-08	199954	24	English	H01L 27/04
	Local appls.: JP1998000337800 Filed:1996-04-30 (98JP-0337800) Div ex JP1996000108998 Filed:1996-04-30 (96JP-0108998)					
	US5926396 =	1999-07-20	199935	56	English	G06F 17/50
	Local appls.: US1996000653651 Filed:1996-05-24 (96US-0653651)					
	TW0305958A =	1997-05-21	199735		XX_XX	G06F 1/32
	Local appls.: TW1996000105339 Filed:1996-05-03 (96TW-0105339)					
	CN1143860A =	1997-02-26	200062		English	H03K 19/00
	Local appls.: CN1996000107886 Filed:1996-05-24 (96CN-0107886)					
	JP09050462A2 =	1997-02-18	199717	38	English	G06F 17/50
	Local appls.: JP1996000108998 Filed:1996-04-30 (96JP-0108998)					

INPADOC Legal Status: Show legal status actions

Priority Number:

Application Number	Filed	Original Title
JP1995000127819	1995-05-26	

Related Accessions:

Accession Number	Type	Derwent Update	Derwent Title
			Semiconductor integrated circuit designing method involves

2003-629309	R	200360	mapping combinational circuit having signal propagation path with signal propagation delay more than design delay upper limit
2000-025274	R	200003	Semiconductor arithmetic circuit having two different voltage levels
2 items found			

Title Terms: LOGIC SYNTHESIS LOW POWER COMBINATION MAP COMBINATION CIRCUIT CIRCUIT DRIVE HIGH LOW VOLTAGE CIRCUIT DELAY ABOVE DESIGN LIMIT CIRCUIT DELAY BELOW LIMIT

Index Terms: SEMICONDUCTOR INTEGRATED CIRCUIT

Hsin-Tien, Taipei 231, Taiwan
(O) 886-2-22185452 Ext.7881
(Fax) 886-2-82186921
minghuichou@via.com.tw

The Delphion Integrated View: INPADOC Record

Title: **CN1143860A: LOGIC SYNTHESIZING METHOD, SEMICONDUCTOR INTEGRATED CIRCUIT AND OPERATIONAL CIRCUIT**

Derwent Title: Logic synthesis for low power combinatorial SIC - involves mapping combinatorial circuit onto circuits driven by high and low voltages when circuit has delay above design limit providing circuit with delay below limit
[Derwent Record]

High
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Country: **CN** China

Kind: **A** Unexamined APPLIC. open to Public inspection

Inventor: **KAZUTAKE OHARA**; Japan

Assignee: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.** Japan
News, Profiles, Stocks and More about this company

Published / Filed: **1997-02-26** / 1996-05-24

Application Number: **CN19969696107886**

IPC Code: IPC-7: **H03K 19/00;**

ECLA Code: None

Priority Number: 1995-05-26 **JP1995000127819**

INPADOC Legal Status: None **Get Now:** Family Legal Status Report

Designated Country: DE FR GB IT NL

Family:

PDF	Publication	Pub. Date	Filed	Title
	US5978573	1999-11-02	1998-10-15	Logic synthesis method, semiconductor integrate circuit and arithmetic circuit
	US5926396	1999-07-20	1996-05-24	Logic synthesis method, semiconductor integrate circuit and arithmetic circuit
☑	JP11274413A2	1999-10-08	1998-11-27	ARITHMETIC CIRCUIT
☑	JP09050462A2	1997-02-18	1996-04-30	LOGICAL SYNTHESIS METHOD, SEMICONDUCTOR INTEGRATED CIRCUIT AN ARITHMETIC CIRCUIT
☑	JP02948524B2	1999-09-13	1996-04-30	
	EP1335309A1	2003-08-13	1996-05-24	Method of designing a semiconductor integrated circuit
	EP0955594A3	2002-04-10	1996-05-24	Arithmetic circuit with two different voltage levels
	EP0955594A2	1999-11-10	1996-05-24	Arithmetic circuit with two different voltage levels
	EP0744704B1	2002-09-18	1996-05-24	Logic synthesis method for designing a semiconductor integrated circuit
	EP0744704A3	1998-04-08	1996-05-24	Logic synthesis method, semiconductor integrate circuit and arithmetic circuit

☑	EP0744704A2	1996-11-27	1996-05-24	Logic synthesis method, semiconductor integrate circuit and arithmetic circuit
☑	DE69623688T2	2003-06-05	1996-05-24	LOGIKSYNTHESEVERFAHREN ZUM ENTWUF INTEGRIERTER HALBLEITERSCHALTUNGEN
	DE69623688C0	2002-10-24	1996-05-24	LOGIKSYNTHESEVERFAHREN ZUM ENTWUF INTEGRIERTER HALBLEITERSCHALTUNGEN
☑	CN1430331A	2003-07-16	2002-11-25	Computing circuit
☑	CN1208900C	2005-06-29	2002-11-25	Computing circuit
☑	**CN1143860A**	1997-02-26	1996-05-24	LOGIC SYNTHESIZING METHOD, SEMICONDUCTOR INTEGRATED CIRCUIT AN OPERATIONAL CIRCUIT
☑	CN1130829C	2003-12-10	1996-05-24	Logic synthesizing method, semiconductor integrated circuit and operational circuit
17 family members shown above				

Other Abstract Info: DERABS G97-001436